Electronic Version
Stylesheet Version v1.1.1

Description

[LIGHT SCATTERING EUVL MASK]

BACKGROUND OF INVENTION

[0001] Field of the Invention

[0002] The invention generally relates to reflective masks, and more particularly to a light scattering and radiation reflective EUVL mask.

[0003] Description of the Related Art

[0004] The optical lithographic technique that is used to image wafers throughout the semiconductor industry relies on transparent masks to transfer an image from the mask to the wafer. As wafer images shrink, new ways of imaging the wafer resist are needed. One likely candidate for the Next Generation Lithography uses Extreme Ultraviolet (EUV) light to image. At the 13.4nm EUV wavelength, materials are too absorptive to build a transmissive mask, so reflective ones are used instead. Conventional Extreme Ultraviolet Lithography (EUVL) masks, such as the mask illustrated in Figure 1, are built by depositing a reflective

film onto an ultra low expansion (ULE) substrate 10. Material properties of ULE substrates are well known in the art. This film can be composed of many different materials. The most commonly deployed reflective Bragg mirror for EUVL mask applications is created with multiple (as many as forty or more) alternating bilayers of molybdenum (Mo) and silicon (Si), finishing with a protective Si cap shown collectively as a Mo/Si multilayer 20. A buffer layer 30 and absorber layer 40 are then deposited on the multilayer stack 20. Additional layers can be deposited anywhere within the capping/buffer/absorber stack for different purposes, such as to provide an etch stop or conductive inspection/repair layer. The mask pattern is written onto a resist layer using standard mask patterning processes. A dry etch transfers the pattern through the absorber layer. Inspection and repair are performed to ensure that the absorber pattern matches the design data and then the final pattern is transferred through the buffer layer to expose the reflective multilayer surface.

[0005] There are many material challenges inherent in building and using an EUVL mask. One fundamental mask issue is the selection of absorber and buffer materials that combine ideal chemical durability, adhesion, dry etch charac-

teristics, and optical. Moreover, maintaining the quality (and hence reflectivity) of the capping layer's reflective surface during mask processing is difficult.

[0006] Generally, conventional optical masks include transmissive regions that permit light to pass onto the wafer and absorptive regions that block the light. However, the masks used in the EUVL system, introduce a new set of challenges. Because an EUVL mask is reflective, the EUV radiation must be exposed to the mask surface at an angle such that the pattern will reflect onto the surface of the wafer. Specifically, light incident on the exposed reflective surface is reflected. Light incident on the patterned absorber film is absorbed, not reflected; an essential component to imaging. A by-product of this absorption is that the radiation heats the mask and must be controlled to avoid pattern distortion and also to limit heat-induced wear that would decrease mask lifetime. Experiments have shown that 5 degrees is the optimal angle of exposure.

[0007] The absorber stack height is finite and creates a shadow under the angle of illumination which blurs the edge of the raised absorber when imaged. This reduction in contrast is a function of the angle of the incident exposure light and both the absorber and buffer layer thickness.

Reduced contrast at the pattern edges is a significant issue since it can result in shifted or mis-sized images on the wafer.

[0008] The industry has sought to overcome these identified challenges, yet a solution has not been adequately defined. Therefore, due to the limitations of the conventional devices and processes, there is a need for a novel EUVL mask which overcomes the problems associated with the standard techniques.

SUMMARY OF INVENTION

[0009] The invention overcomes the above-identified problems by eliminating both the buffer and absorber layers of the mask stack entirely. The invention provides a light scattering extreme ultraviolet lithography mask wherein a silicon molybdenum multilayer is deposited over a patterned blank with specific topography that causes the EUV radiation to be reflected in areas where the exposure light is intended to impinge on the wafer and scattered in areas where the light is not intended to reach the wafer. The topography in the regions intended to reflect light onto the wafers are configured as flat regions. However, in regions where the EUV radiation is not intended to reach the surface of the wafer, the topography is configured such that

it scatters the radiation out of the imaging optics of the stepper and hence would not print.

[0010] Specifically, the invention provides an extreme ultraviolet lithography mask comprising an ultraviolet reflective region and an ultraviolet scattering region, wherein the reflective region and the scattering region are comprised of the same material. The reflective region comprises a molybdenum and silicon multilayer, wherein the multilayer comprises a flat surface configured to reflect incoming ultraviolet radiation waves for imaging on a semiconductor wafer. The scattering region comprises a molybdenum and silicon multilayer, wherein the multilayer comprises one or more sloped surfaces configured at an angle chosen to deflect incoming ultraviolet radiation waves to prevent/avoid collection by the exposure optics and to prevent imaging onto a semiconductor wafer, wherein the angle is greater than a collection angle of the exposure optics. In alternate embodiments, the scattering region comprises a roughened surface, a jagged surface, or a curved surface configured to deflect incoming ultraviolet radiation waves to prevent/avoid collection by the exposure optics and to prevent printing onto a semiconductor wafer.

[0011] Moreover, the invention provides a light scattering reflective mask comprising an ultra low expansion substrate, a crystalline silicon layer on top of the ultra low expansion substrate, and a radiation reflecting and light scattering multilayer comprising molybdenum and silicon on top of the crystalline silicon layer. The multilayer conforms to the underlying silicon layer to have a level portion and an uneven portion. The level portion is configured to reflect incoming ultraviolet radiation waves onto a semiconductor wafer. In one embodiment, the uneven portion comprises a sloped configuration arranged at an angle to deflect incoming ultraviolet radiation waves to prevent light from reaching the semiconductor wafer. In another embodiment, the uneven portion comprises a roughened surface configured to deflect incoming ultraviolet radiation waves to prevent/avoid collection by the exposure optics and to prevent printing onto a semiconductor wafer. In yet another embodiment, the uneven portion comprises a jagged surface configured to deflect incoming ultraviolet radiation waves to prevent/avoid collection by the exposure optics and to prevent printing onto a semiconductor wafer. Alternatively, the uneven portion comprises a curved surface configured to deflect incoming ultraviolet

radiation waves to prevent/avoid collection by the exposure optics and to prevent printing onto a semiconductor wafer.

[0012] Another aspect of the invention provides a method of forming an extreme ultraviolet lithography mask by anodically bonding a crystalline silicon layer on top of an ultra low expansion substrate, and then depositing a conformal multilayer comprising molybdenum and silicon on top of the crystalline silicon layer, wherein the multilayer comprises a surface having a level portion to reflect light onto the wafer and an uneven portion to scatter light so that it does not impinge on the wafer. Prior to the step of depositing the reflective multilayer, the method further comprises depositing a hardmask over the crystalline silicon layer, depositing a photoresist mask over the hardmask, creating a pattern in the photoresist mask, and transferring the pattern to the hardmask. The method further comprises etching the crystalline silicon layer to produce an uneven surface in etched regions of the crystalline silicon layer, and removing the hardmask. Additionally, the pattern is transferred to the hardmask using a plasma etch, wherein the etching of the crystalline silicon comprises an anisotropic wet etch, which is performed

using an alkaline solution such as aqueous potassium hydroxide (KOH), tetramethylammonium hydroxide (TMAH), or ethylene diamine pyrocatechol (EDP). Furthermore, the etching is performed along <100> lattice planes of the crystalline silicon layer.

[0013] Moreover, the level regions are configured to reflect incoming ultraviolet radiation waves for printing a semiconductor wafer, and in a first embodiment, the uneven regions comprises sloped surfaces conformal to the underlying crystalline silicon layer, wherein the sloped surfaces are configured at an angle to deflect incoming extreme ultraviolet radiation waves to prevent printing to a semiconductor wafer, wherein the angle is 54 degrees from normal. In a second embodiment, the method comprises configuring the uneven portion to have a roughened surface to deflect incoming ultraviolet radiation waves to prevent printing to a semiconductor wafer. In a third embodiment, the method comprises configuring the uneven regions to have a jagged surface to deflect incoming ultraviolet radiation waves to prevent printing to a semiconductor wafer. In another embodiment, the method comprises configuring the uneven regions to have a curved surface to deflect incoming ultraviolet radiation waves to

prevent printing to a semiconductor wafer.

[0014] The invention eliminates the need for a buffer or absorber layer within the mask stack and overcomes the problems inherent with conventional EUVL masks previously described. Because the multilayer is deposited as the final step in the mask fabrication, the multilayer will not be subjected to the plasma etches, wet etches, and multiple cleans that degrade the multilayer in the standard EUVL mask process and consequently reduce the mask reflectivity. In this invention, the higher reflectivity increases the mask contrast between reflective and scattering regions, decreases the required exposure time, and reduces the amount of radiation that is absorbed by the mask.

[0015] The inventive mask comprises a substrate (which may include a bonded crystalline Si layer) and the multilayer without an absorber or buffer layer. The absence of a raised absorber stack eliminates the shadow effect during wafer printing. This results in an abrupt transition from dark to reflective mask regions and the effect is an improvement in the edge contrast on the lithographic wafer.

[0016] These and other aspects of the invention will be better appreciated and understood when considered in conjunction with the following description and the accompanying

drawings. It should be understood, however, that the following description, while indicating preferred embodiments of the invention and numerous specific details thereof, is given by way of illustration and not of limitation. Many changes and modifications may be made within the scope of the invention without departing from the spirit thereof, and the invention includes all such modifications.

Brief Description of Drawings

[0017] The invention will be better understood from the following detailed description with reference to the drawings, in which:

[0018] Figure 1 is a schematic cross-sectional diagram of a conventional EUVL mask;

[0019] Figure 2 is a schematic cross-sectional diagram of an EUVL mask according to an embodiment of the invention;

[0020] Figure 3(a) through 3(e) are schematic cross-sectional diagrams illustrating sequential processing steps in the manufacturing of an EUVL mask according to an embodiment of the invention;

[0021] Figure 4 is a schematic cross-section diagram of a EUVL mask according to an alternate embodiment of the invention; and

[0022] Figures 5(a) and 5(b) are flow diagrams illustrating preferred methods of the invention.

DETAILED DESCRIPTION

[0023] The invention and the various features and advantageous details thereof are explained more fully with reference to the non-limiting embodiments that are illustrated in the accompanying drawings and detailed in the following description. It should be noted that the features illustrated in the drawings are not necessarily drawn to scale. Descriptions of well-known components and processing techniques are omitted so as to not unnecessarily obscure the invention. The examples used herein are intended merely to facilitate an understanding of ways in which the invention may be practiced and to further enable those of skill in the art to practice the invention. Accordingly, the examples should not be construed as limiting the scope of the invention.

[0024] As previously mentioned, there is a need for a novel EUVL mask and method of manufacturing an EUVL mask, which overcomes the problems associated with the standard masks and associated manufacturing techniques. Referring now to the drawings, and more particularly to Figures 2 through 5(b), there are shown preferred embodiments

of the invention.

[0025] In a first embodiment, the invention provides an EUVL mask that has partially sloped surfaces configured as sloped sidewalls as depicted in Figure 2. While not explicitly shown in the figures, those skilled in the art would readily understand that the sloped sidewalls could be configured to be generally curvilinear (either convexly or concavely) shaped. As illustrated in Figure 2, the incoming EUV radiation at 5 degrees is depicted as the solid arrows, and normal EUV reflection is shown as the dashed arrows. The radiation that is reflected off of the flat surface of the multilayer 160, shown with the dashed arrows, will be printed on the wafer. In the patterned areas with the sloped sidewalls, the radiation is deflected at an angle that will not print on the wafer. The out of plane reflections are depicted as the dotted arrows in Figure 2.

[0026] The invention configures a ULE substrate 100 with a layer of crystalline silicon 110.

[0027] Figures 3(a) through 3(e) illustrate the sequential processing steps involved in manufacturing an EUVL mask according to the invention. Preferably, the invention joins a layer of crystalline silicon 110 on a quartz substrate 100 by anodically bonding a silicon wafer to quartz as shown

in Figure 3(a). Anodic bonding is a process well-known to those skilled in the art, and may include the general process described in U.S. Patent No. 6,368,942, the complete disclosure of which, in its entirety, is herein incorporated by reference.

[0028] The next steps of the invention involve depositing a hardmask 120 and resist 130 upon the crystalline silicon layer 110 as shown in Figure 3(b). Then, as illustrated in Figure 3(c), the desired pattern is written in the resist 130 and the pattern is transferred to the hardmask 120 through a plasma etch. This creates opened regions (openings) 140 in the hardmask 120, wherein the openings 140 are patterned down to the surface 115 of the underlying crystalline silicon 110.

[0029] The next step, as shown in Figure 3(d), is to wet etch the crystalline silicon 110 anisotropically, preferably with a wet etch solution, such as aqueous potassium hydroxide (KOH), tetramethylammonium hydroxide (TMAH), or ethylene diamine pyrocatechol (EDP). The silicon 110 is etched along the <100> lattice planes preferably giving approximately a 54 degree sidewall slope of crystalline silicon 110 in the opened regions 140 (thereby resulting in opened sloped regions 155) defined by the crystalline sili-

con 110, thereby resulting in sloped sidewalls 150. The <111> crystal plane of crystalline silicon etches much more slowly that the other crystal planes of silicon in alkaline solutions by at least a factor of 100 (more slowly). Hence, in <100> silicon, sloped sidewalls 150 with an angle of 54 degrees result because the <111> plane does not etch as fast as the other crystal planes. Ultimately, if the features are small enough or the silicon thick enough, the reaction is self-terminating. For instances where there are large regions of open space which are required to absorb or scatter the incident EUVL light, this pattern can be repeated. This creates multiple "wells" that act together to reflect the EUV light out of the focal plane.

[0030] After the hardmask 120 is stripped, a Mo/Si multilayer 160 is deposited over the crystalline silicon layer 110 and is filled into the opened sloped region 155 of the crystalline silicon layer 110. As shown in Figure 3(e) the Mo/Si multilayer 160 assumes the configuration of the underlying etched crystalline silicon layer 110 and includes sloped regions 165 having sloped sidewalls 180 configured above the underlying sloped region 155 of the crystalline silicon layer 110. Accordingly, the Mo/Si multilayer 160 completely fills the sloped region 155 the crystalline

silicon layer 110. Furthermore, the Mo/Si layer 160 further comprises selective flat (level) surfaces 170 configured in between the uneven surfaces (uneven regions) 165.

[0031] Additionally, as shown in Figure 3(e), the sloped sidewalls 180 are configured at an angle θ which will allow deflection of incoming ultraviolet radiation waves in order to prevent collection by exposure optics and to prevent printing onto a semiconductor wafer, wherein the angle θ is greater than a collection angle of the exposure optics. In one embodiment, the angle is created by etching the crystalline silicon layer 110 at an angle of θ that is 54 degrees from normal. The reflective multilayer is conformal to the underlying crystalline silicon 110 and matches the 54 degree. Figure 4 illustrates an alternate embodiment of the invention, wherein the uneven portion 190 of the Mo/Si multilayer 160 is formed by roughening the surface 170 of the Mo/Si multilayer 160. Techniques that include reactive ion etching or wet etching can be used to roughen the surface 170. As shown in the magnified view within the dashed oval circle in Figure 4, the uneven portion 190 may be configured as a jagged surface. The jagged surface can be defined as any roughness that deviates significantly from the target specification of < 0.15 nm RMS

(root mean square) surface roughness. A roughness of approximately 10 nm would prevent effective reflection of incident EUV radiation. The roughness is analogous to a micro version of the sloped surface that can be created with the anisotropic wet etching of silicon described above, and serves the same purpose on a smaller scale.

[0032] In Figures 5(a) and 5(b) flow diagrams illustrating preferred methods of forming an EUVL mask according to the invention are described. Generally, as provided in Figure 5(a), a method of forming an EUVL mask comprises forming 200 a radiation reflective region 170 on a surface of the mask, and forming 210 a light scattering region 165, 190 on the surface of the mask, wherein the radiation reflective region 170 and the light scattering region 165, 190 are comprised of the same material (Mo/Si) 160.

[0033] More specifically, as shown in Figure 5(b), the method of forming an EUVL mask according to the first embodiment of the invention comprises depositing 300 a crystalline silicon layer 110 over an ULE substrate 100, depositing 210 a hardmask 120 over the crystalline silicon layer 110, depositing 320 a photoresist mask 130 over the hardmask 120, creating 330 a pattern in the photoresist mask 130, transferring 340 the pattern to the hardmask 120, etching

350 the crystalline silicon layer 110 to produce sloped sidewalls 180 in etched regions 165 of the crystalline silicon layer 110, removing 360 the hardmask 120, and depositing 370 a Mo/Si layer 160 over the crystalline silicon layer 110. The Mo/Si layer 160 further comprises flat surfaces 170 configured to reflect incoming extreme ultraviolet radiation waves for printing a semiconductor wafer. Additionally, the Mo/Si layer 160 further comprises sloped sidewalls 180 corresponding to the sloped sidewalls 150 of the crystalline silicon layer 110. Furthermore, the sloped sidewalls 180 of the Mo/Si layer 160 are configured at an angle of at least 54 degrees from normal to deflect incoming extreme ultraviolet radiation waves to prevent printing to a semiconductor wafer.

[0034] The invention eliminates the need for a buffer or absorber layer within the mask stack and overcomes the problems inherent with conventional EUVL masks previously described. Because the multilayer is deposited as the final step in the mask fabrication, the multilayer will not be subjected to the plasma etches, wet etches, and multiple cleans that degrade the multilayer and consequently reduce the mask reflectivity. This higher reflectivity increases the mask contrast between reflective and scatter-

ing regions, decreases the required exposure time, and reduces the amount of radiation that is absorbed by the mask. Stepper throughput is the number of wafers that can be printed in a given time period, such as wafers/hour. Decreasing exposure time increases as described above directly increases stepper throughput.

[0035] Moreover, the inventive mask comprises a substrate 100 (which may include a bonded crystalline Si layer) and a multilayer 160 formed without an absorber or buffer layer. The absence of a raised absorber stack eliminates the shadow effect during wafer printing. This results in an abrupt transition from dark to reflective mask regions and the effect is an improvement in the edge contrast on the lithographic wafer. An additional advantage achieved by the invention is that the radiation is reflected so that there is less heating of the EUVL mask, which is a significant concern for image control and lifetime.

[0036] Generally, the invention includes a novel mask including an absorbing region 110 that is created before the Mo/Si multilayer 160 is deposited. The patterning can be achieved by either roughening the surface of the mask in regions 190 where the EUV light is not intended to reach the printed wafer surface or forming a grid of sloped

sidewalls 180 in the regions 165 where the EUV light is not intended to reach the printed wafer surface. Techniques that include reactive ion etching or wet etching techniques can be used to either roughen the surface 190 or create the sloped sidewalls 180. The level pattern 170 that is to be reflected to the printed wafers surface will remain smooth and planar. After multilayer deposition 370, the uneven patterned areas 165, 190 act as the absorber of the EUVL mask because the reflective capabilities of the Mo/Si film 160 are locally destroyed. However, as described above, these regions 165, 190 do not actually absorb the EUV radiation but rather deflect the EUV radiation at an angle that will not develop the photoresist on the wafer.

[0037] The foregoing description of the specific embodiments will so fully reveal the general nature of the invention that others can, by applying current knowledge, readily modify and/or adapt for various applications such specific embodiments without departing from the generic concept, and, therefore, such adaptations and modifications should and are intended to be comprehended within the meaning and range of equivalents of the disclosed embodiments. It is to be understood that the phrases or terminology em-

ployed herein is for the purpose of description and not of limitation. Therefore, while the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.